REMARKS

As a preliminary matter, Applicant respectfully requests an updated copy of the Form PTO-1449 indicating consideration of the references listed under "Other Documents" section of the form submitted with an IDS filed July 11, 2001.

The title and the abstract have been amended as required.

Claims 1-15 stand rejected under 35 U.S.C. 101 as being directed to non-statutory subject matter. Applicant respectfully traverses at least with respect to claim 1. Claim 1 is directed to a processor which is clearly a statutory subject matter. In any event, claims 1, 14 and 15 have been amended in a readily apparent manner to address this rejection and to expedite prosecution.

Claim 1 stands rejected under 35 U.S.C. 112, first paragraph. Applicant respectfully disagrees with the Examiner that the "claimed invention is not supported by either a specific and substantial asserted utility." The specification of the present application does, in fact, explain the utility of the invention. The Examiner is referred to page 3, line 34 to page 4, line 3; page 5, lines 10 to 15; page 13, line 34 to page 14, line 14; and page 14, lines 28 to 32, for example. For purposes of expediting prosecuting, claim 1 has been amended in a readily apparent manner to overcome this rejection. Withdrawal of the rejection is respectfully requested

Claims 1-13 stand rejected under 35 U.S.C. 112, second paragraph, as being indefinite. Claims 1, 3 and 9 have been amended to overcome this rejection. Claim 4 has been canceled. Withdrawal of this rejection is respectfully requested.

Claims 1-4 and 9-15 stand rejected under 35 U.S.C. 102(b), as being anticipated by Kissell. Claims 2 and 4 have been canceled. Features of claim 2 have been incorporated in independent claims 1, 14 and 15. Applicant respectfully traverses this rejection, because the cited reference does not disclose (or suggest) that *for every one of the first operations (i.e. the operations which are specifiable in either external format) which the processor is capable of executing,* the instruction specifying that operation in the first external format is identical, in each of the common opcode bits, to the instruction specifying that operation in the second external format, as now recited in claims 1, 14 and 15.

The Kissell paper ("MIPS16: High-density MIPS for the embedded market") discloses a processor adapted to receive instructions in one of first and second instruction formats. Following *arguendo* the same interpretation of Kissell as the Examiner in paragraph 24 of the Office Action, the first external instruction format will be taken as the 16-bit format MIPS16, and the second external instruction format will be taken as one of the 32-bit MIPS instruction formats, for example MIPS-I. The processor internally executes instructions in the 32-bit format, which therefore constitutes an internal instruction format. Instructions received in the first (MIPS16) external format are translated into 32-bit MIPS instructions. It also appears that certain operations cannot be specified in the first (MIPS16) external format, for example due to space limitations in that format.

The Examiner has relied on the further reference "Product Description: MIPS application-specific extension", as showing the definition of the opcodes in Kissell. The Product Description document shows that the preselected opcode bits in which the opcode

appears in the MIPS16 instruction are the bits 11 through 15. In the 32-bit MIPS instruction the preselected opcode bits in which the opcode appears are bits 26 through 31. In the case of the Load Byte (LB) instruction shown on page 26 of the Product Description document, the opcode bits 11 through 15 ("10000") are identical to the 5 most significant bits (bits 27 through 31) of the opcode bits 26 through 31 of the 32-bit MIPS instruction ("100000"). Thus, the requirement of the original claim 1 for one "first operation" to have identical "common opcode bits" in the first and second external formats is arguably satisfied by this particular Load Byte example.

However, the claims, as amended, now require that *for every one of the first operations (i.e. the operations which are specifiable in either external format) which the processor is capable of executing,* the instruction specifying that operation in the first external format is identical, in each of the common opcode bits, to the instruction specifying that operation in the second external format. This feature is not disclosed (or suggested) in the cited reference. For this reason, claims 1, 14 and 15, and claims 3 and 5-13 which depend from claim 1, are now believed to be allowable.

To further assist in understanding the reference and the present invention, Applicant observes that it would be possible to choose any suitable set of 5 bits from amongst the bits 26 through 31 in the 32-bit MIPS instruction as the common opcode bits. For example, the bits could be chosen as the bits 26, 27, 28, 30 and 31. In this case, the LB instruction in the 32-bit instruction format could be formed by taking the 5 opcode bits ("10000") from 11 through 15 in the LB MIPS16 instruction, mapping them respectively to

bits 26, 27, 28, 30 and 31, and setting bit 29 to "0", since this also produces, as bits 26 through 31 of the 32-bit MIPS instruction, the opcode "100000". This mode of translation would even hold good for the subsequent LBU, LH, LHU and LW instructions. However, it breaks down for other subsequent instructions, for example the Store Byte instruction SB shown on page 32. In this case, the translation of the SB MIPS16 instruction ("11000") produces the opcode "110000", whereas the correct opcode for the SB 32-bit MIPS instruction is "101000" as shown on page 32 of the Product Description. Thus, whatever choice of common opcode bits is made in the Product Description document, the requirement of the amended claim 1 for the common opcode bits to be identical is not met for *every* available first operation.

The significance of this is that in the MIPS processor, the conversion from MIPS16 format into 32-bit MIPS instruction format cannot be independent of the operation specified by the external format instruction. In other words, a different translation operation is required for the SB operation compared to the LB operation. Accordingly, the instruction translation unit in the MIPS processor is more complicated and hence either functions more slowly or utilizes more computational resources than the instruction translation unit in the present invention. For example, it appears that the instruction translation unit in the MIPS processor may need to partially decode the instruction to translate it and/or may need to use some form of lookup table. In the present invention, on the other hand, because the common opcode bits are identical for every first operation, no such decoding or lookup table is necessary.

When all of the available first operations set out in the Product Description document are considered (i.e. pages 26 to 66 of the Product Description), rather than just the particular LB example in isolation, it is clear that the requirement that *for every one of the first operations which the processor is capable of executing* the instruction specifying that operation in the first external format is identical, in each of the common opcode bits, to the instruction specifying that operation in the second external format, is not satisfied by the cited reference.

Claims 5-8 stand rejected under 35 U.S.C. 103(a), as being unpatentable over Kissell. Applicant respectfully traverses this rejection for the reasons given above traversing the rejection of claim 1, from which these claims depend, and because of the additional features that they recite.

New claim 30 describes features similar to claims 14 and 15, but in a propagated signal format. It is also believed to be allowable.

For all of the above reasons, Applicants request reconsideration and allowance of the claimed invention. The Examiner should contact Applicants' undersigned attorney if a telephone conference would expedite prosecution.

Respectfully submitted,

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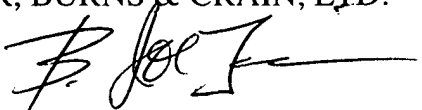
By 

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